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(54) Clock recovery for ATM receiver

(57) Clock recovery circuit for an ATM receiver. Automatically derive the frequency of the source signal which is transmitted by the ATM cells. A subcircuit (3, 4, 5) determines, on the basis of the cell rate, the nominal bit rate of the source signal and generates a clock signal having a frequency which is consistent therewith. A second subcircuit (6, 7, 8, 9, 10) corrects, in proportion to the difference between the nominal bit rate and the mean actual bit rate, the frequency of the clock signal generated by the first subcircuit.

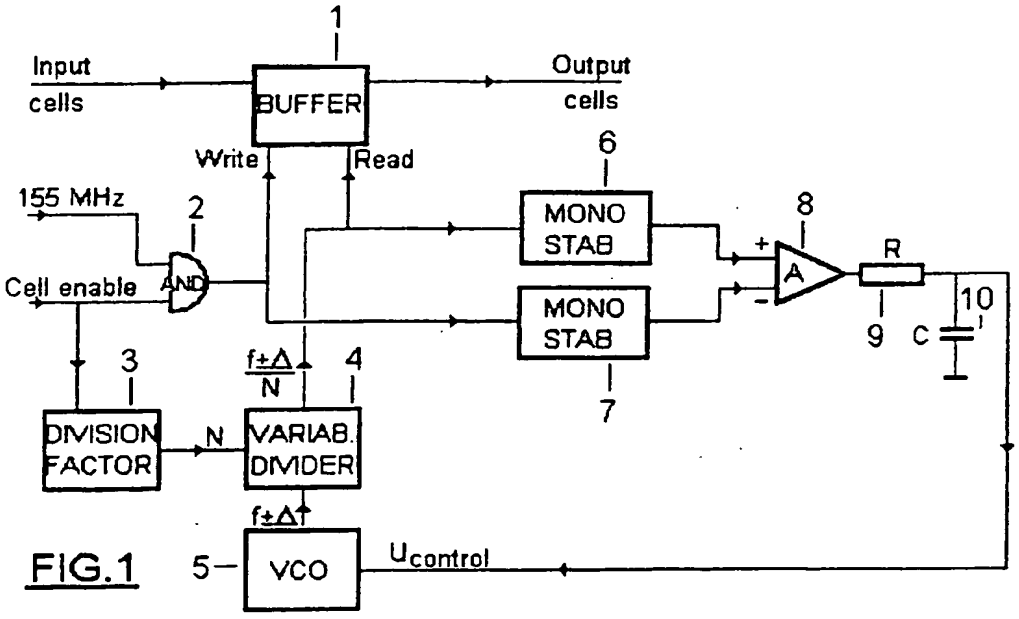


FIG.1

EP 0 705 051 A1

Description

A. BACKGROUND OF THE INVENTION

The invention relates to an ATM receiver, in particular the clock recovery circuit.

In an ATM transmission system it is possible to transmit, via various virtual channels, source signals at different bit rates, as a result of which the number of ATM cells per unit time, the cell rate, may differ in the one virtual channel from that in another channel. Where the cells of a particular channel arrive at a receiver - allocated temporarily to said channel - said cells must, after having been incorporated in a buffer, be read out therefrom at a clock frequency which is consistent with the cell rate of that channel and with the bit rate (and clock frequency) of the source signal.

The subject of the present invention is a circuit for deriving, from the cell arrival times, the clock frequency at which said buffer is read out. In the process it is necessary to allow for different nominal cell rates and for variations within those nominal cell rates. So far, the objective of detecting, in a satisfactory manner and entirely automatically, the clock frequency from the arrival times of ATM cells has not been met with a known solution.

B. SUMMARY OF THE INVENTION

The invention comprises a clock recovery circuit for an ATM receiver, the clock frequency being derived entirely automatically from the cell arrival times. To this end, the circuit according to the invention comprises first means for determining, on the basis of the cell rate of the received cells, the nominal bit rate of the source signal and generating a clock signal having a frequency which is consistent therewith, and second means for correcting, in proportion to the difference between the nominal bit rate determined by the first means and the mean actual bit rate, the frequency of the clock signal generated by the first means. The invention will be expounded hereinafter with reference to a number of figures.

C. ILLUSTRATIVE EMBODIMENTS

Figure 1 shows an illustrative embodiment of the invention. Figure 2 depicts a number of signals. Figure 3 shows an illustrative embodiment of one of the units shown in Figure 1.

The circuit shown in Figure 1 has been designed for automatic recovery of the source clock for source signals having bit rates of 64, 128, 144, 192, 256, 512, 1024 and 2048 kbits/sec. ATM cells are fed to a buffer 1 via an input circuit. By an AND gate 2, a WRITE signal is composed for the cell buffer 1 from a network clock signal of 155.520 MHz (current standard for ATM networks) and a "cell enable" signal by means of which an ATM cell is admitted by the input circuit to buffer 1. Such a "cell enable" signal is produced, for example, by an access monitoring unit such as that described in patent EP - 381 275 B1 in the name of Applicant. The WRITE signal has a "burst" character (see also Figure 2). The rest of the circuit serves to produce a READ clock signal which corresponds to the cell rate of the cells presented to buffer 1 and which does not have a burst character (see also Figure 2). The frequency of that READ signal is equal to the bit rate of the source signal and therefore equal to the frequency of the source clock.

The circuit includes a coarse adjustment for the clock frequency at which buffer 1 is read out, comprising a division factor adjustment 3 and a variable frequency divider 4. The circuit further includes a fine adjustment, comprising monostable multivibrators 6 and 7, an amplifier 8, a low-pass filter 9, 10 and a VCO (Voltage Controlled Oscillator).

The division factor adjustment 3 is driven by the "cell enable" signal. After the time between two (or more) successive "cell enable" signals has been measured and the measured time has been categorized in accordance with the closest standard time which corresponds to one of the abovementioned bit rates, a division factor N which has been allocated to that closest standard time is presented to the frequency divider 4. The frequency divider 4 divides the frequency of the clock signal which is presented by the VCO 5 by factor N.

The variation in cell arrival times (see also Figure 3) must be compensated for by a fine adjustment. To this end, the WRITE signal is also presented to a monostable multivibrator 7, which assigns a defined width to the WRITE pulses presented. The READ signal is presented to a monostable multivibrator 6 which ensures that the READ pulses are assigned a defined width. The two signals then pass to the + and - input, respectively, of an amplifier 8. At the output a capacitor 10, via a resistor 9, is charged by the READ pulses and discharged by the WRITE pulses. In the case of equilibrium between the number of cells written to the buffer and the number of cells read out, there is equilibrium between charging and discharging of the capacitor 10. If the number of WRITE pulses increases with respect to the number of READ pulses, the voltage $U_{control}$ over capacitor 9 drops, and the frequency of the VCO 5 is readjusted, as a result of which the READ clock frequency increases.

Figure 3 shows a specific embodiment of the abovementioned unit 3 which calculates the division factor N. This unit comprises a NAND gate 11, a clock generator 12 and a counter 13. Counter 13 receives pulses from clock generator 12 during the period when there is no "cell enable" signal (see also Figure 2). If the cell rate is low, that period is relatively long and the counter attains a relatively high value; at a high cell rate, the counter reaches only a low value. The counter value reached is presented to a number of digital comparators 14 which are each set to a counter value which represents a specific nominal bit rate. The comparator 14 which has a counter value which is closest to the counter value reached by the counter 13 gives an indication to processor 15. Processor 15 calculates, on the basis of the posi-

tion of that comparator, the value for N and passes this to the variable divider 4. In the case of a low cell rate, the counter 13 reaches a relatively high value, and the value of N likewise becomes relatively high, as a result of which the value of f+Δ/N is relatively low.

D. References

EP 0 381 275 B1 in the name of KONINKLIJKE PTT NEDERLAND N.V.

Claims

1. Clock recovery circuit for an ATM receiver, for automatically deriving, from the cell rate of received ATM cells, the clock frequency of the source signal which is transmitted by the ATM cells, characterized by first means for determining, on the basis of the cell rate of the received cells, the nominal bit rate of the source signal and generating a clock signal having a frequency which is consistent therewith, and second means for correcting, in proportion to the difference between the nominal bit rate and the mean actual bit rate of the received cells, the frequency of the clock signal generated by the first means.

2. Clock recovery circuit according to Claim 1, characterized in that said first means comprise a division factor unit (3) for determining, on the basis of two or more successive cell arrival times, the nominal bit rate of the source signal transmitted by the ATM cells and generating a division factor (N) as a function of that nominal bit rate, together with a frequency divider (4) for dividing the frequency (f) of a clock signal, which has been output by a clock generator (5), by said division factor.

3. Clock recovery circuit according to Claim 2, characterized by second means which, in proportion to, on the one hand, the number of cell bits received over a period of two or more successive cell arrival time and, on the other hand, the number of clock pulses output by the frequency divider (4) over that same period, output a frequency control signal ($U_{control}$) to said clock generator (5).

4. Clock recovery circuit according to Claim 3, characterized in that clock pulses are presented, in proportion to the cells bits received, to a monostable multivibrator (7) and that the clock pulses output by the frequency divider (4) are presented to an identical monostable multivibrator (6), the output of both said monostable multivibrators being connected to the positive and negative input, respectively, of an amplifier (8) whose output is connected via an integration circuit (9, 10) to the frequency control terminal of a voltage-controlled oscillator (5).

5. Clock recovery circuit according to Claim 1, characterized in that the cell bits of an ATM cell arriving at the receiver are written to a buffer (1) under the control of the network clock signal, while said buffer is read out under the control of the clock signal generated by the first means.

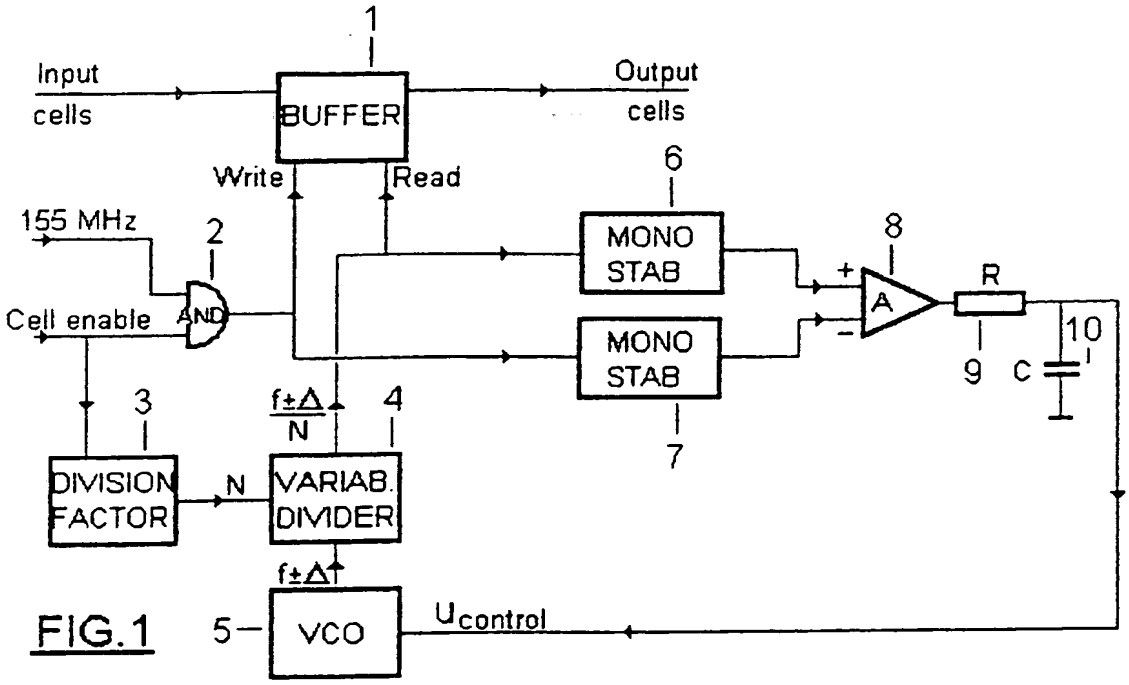

1
Input
cells
BUFFER
Output
cells
Write
Read
6
155 MHz
2
MONO
STAB
8
+
A
R
Cell enable
AND
MONO
STAB
−
9
C
10
3
f±Δ
N
4
7
DIVISION
FACTOR
N
VARIAB.
DIVIDER
f±Δ
5
VCO
Ucontrol

FIG.1

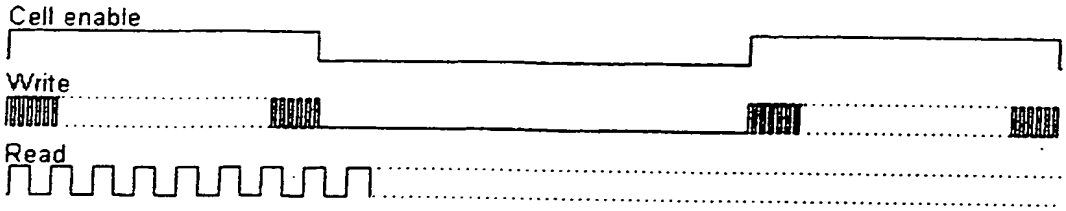
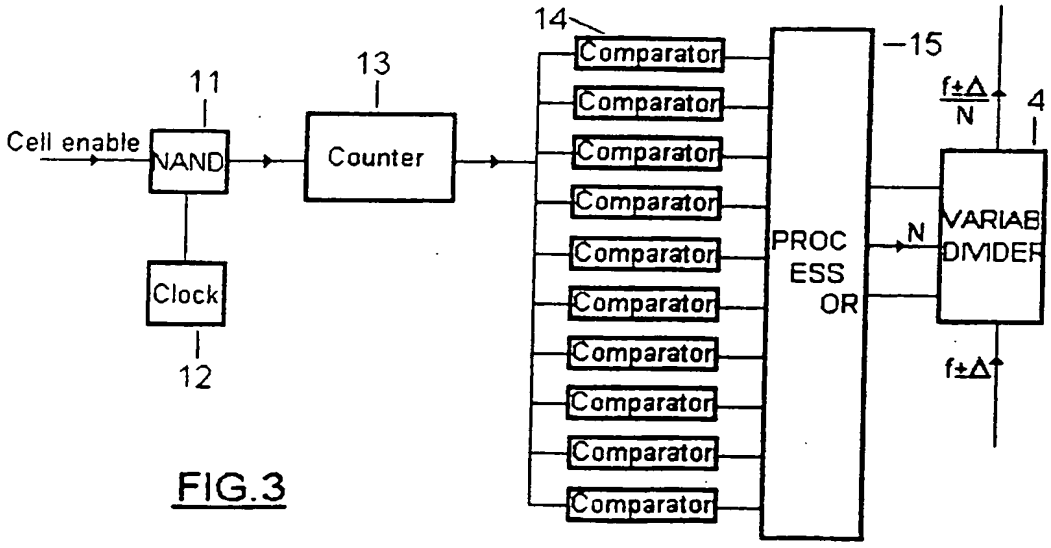

Cell enable
Write
Read

FIG.2


14
Comparator
Comparator
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Comparator
Comparator
Comparator
Comparator
Comparator
Comparator
Comparator
15
PROC
ESS
OR
f±Δ
N
4
N
VARIAB
DIVIDER
f±Δ
13
Counter
11
Cell enable
NAND
Clock
12

FIG.3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 20 2376

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	OPTICAL ENGINEERING, vol. 28, no. 7, July 1989 BELLINGHAM US, pages 781-788, XP 000033802 H.J.CHAO,C.A.JOHNSTON 'Asynchronous transfer mode packet video transmission system.' * page 785, left column, line 18 - page 786, left column, line 28 *	1,2,5	H04Q11/04 H04J3/06 H04L7/02
A	US-A-4 105 946 (SANSUI ELECTRIC CO., LTD.) 8 August 1978 * column 1, line 5 - line 35 *	1-5	
A	EP-A-0 577 329 (AMERICAN TELEPHONE AND TELEGRAPH COMPANY) 5 January 1994 * column 1, line 55 - column 2, line 21 *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H04Q
H04J
H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 December 1995	Veen, G

CATEGORY OF CITED DOCUMENTS

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& : member of the same patent family, corresponding document

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